REMARKS

Upon entry of this amendment, which amends claims 1-6, claims 1-6 remain pending, and newly added claims 7-18 are presented for examination. Claim 1 was rejected under 35 U.S.C. §102(a) as being anticipated by Applicant's admitted prior art. Claims 2-6 were objected to as being dependent on a rejected base claim, but were found to be allowable if rewritten in independent form. Reconsideration in view of the foregoing amendments and following remarks is respectfully requested.

Attached hereto is a "Version with Markings to Show Changes Made," indicating the changes that were made in the specification and claims.

Amendments to the Specification

The specification has been amended to correct various informalities discovered therein, as shown in the "Version with Markings to Show Changes Made." It is respectfully submitted that no new matter has been added.

Amendments to the Drawings

Applicant submits herewith an amended drawing sheet indicating in red ink proposed amendments to Fig. 4. Labels for the output signal lines have been corrected to conform to the specification, in particular, at p. 7, lines 17-27, and p. 6, lines 10-17, as well as to the signals shown in Fig. 3. It is respectfully submitted that these proposed changes do not add new matter.

Rejection of Claim 1

Claim 1 was rejected under 35 U.S.C. §102(a) as being anticipated by Applicant's admitted prior art, specifically Figure 2 of the present application. Applicant respectfully traverses, in view of the amendment to claim 1. As amended, claim 1 recites a delay locked loop having a delay chain means, a comparison means, and "an instant locking delay control means for detecting whether a locking between the reference clock signal and the delayed clock signal is accomplished." When locking is detected, "the instant locking delay control means is operated to compensate for noise detected by the

comparison means and to control the controllable delay chain means." When locking is not detected, "the instant locking delay control means is not operated to compensate for noise"; instead, "the output signals generated by the comparison means are used to directly control the controllable delay chain means."

The circuit recited in claim 1 differs from the circuit shown in Figure 2 in at least two ways. First, the delay locked loop of Figure 2 lacks the "instant locking delay control means" as recited in amended claim 1 because the circuit of Figure 2 does not include any component that "detect[s] whether a locking between the reference clock signal and the delayed clock signal is accomplished." Second, in the circuit of Figure 2, there is no circumstance in which the output of the comparison block 210 is used directly to control the delay chain block 200. Instead, the delay chain block 200 is always controlled by signals generated by the careful delay controller 220. Nothing in Figure 2 or the accompanying description suggests that the output of the careful delay controller 220 could be selectively bypassed in favor of using the output of the comparison block 210 directly.

For at least these reasons, Applicant respectfully submits that claim 1 is patentable over the circuit of Figure 2. Withdrawal of the rejection of claim 1 under 35 U.S.C. §102(a) is respectfully requested.

Objection to Claims 2-6

Claims 2-6 were objected to as being dependent on a rejected base claim, but were found to be allowable if rewritten in independent form. In view of the amendment to claim 1 and the foregoing remarks, Applicant respectfully submits that claims 2-6 are in condition for allowance without being rewritten in independent form. Withdrawal of the objection is respectfully requested.

Amendments to Claims 2-6

Applicant notes for the record that claims 2-6 have been amended to correct minor informalities therein. Claim 2 has been amended to correct minor grammatical errors and to replace the pronoun "that" with the corresponding antecedent.

Claim 2 has also been amended to provide clear antecedent basis for terms used therein. In each of claims 3-6, "contains" has been replaced by "comprises" to more clearly indicate the open-ended nature of the claims. In claim 4, minor typographical errors have been corrected, and the claim has been amended to provide clear antecedent basis for terms used therein. Grammatical errors were corrected in claims 5 and 6. It should be noted that these amendments are not intended to narrow the scope of the claims.

New Claims

Claims 7-18 have been added by this amendment. It is respectfully submitted that support for these claims may be found throughout the specification. Independent claims 7 and 15 are supported, e.g., by Figures 3 and 4 and accompanying disclosure. Dependent claims 8-14 and 16-18 are supported by Figures 5-10 and accompanying disclosure.

To expedite prosecution, it is respectfully submitted that claims 7-18 are patentable over the circuit of Figure 2.

Independent claim 7 recites a delay control circuit for a delay locked loop. The control circuit has a time-offset detector "configured to generate a first adjustment signal indicating a need for an increase or decrease of the delay time," and a delay controller "configured to generate a second adjustment signal by applying noise compensation to the first adjustment signal." A locking detector is "configured to assert a lock signal when a locking condition is satisfied," and a selector is "configured to provide one of the first and second adjustment signals as the control signal." Thus, when a locking condition is satisfied, a noise-compensated adjustment signal is used to control the delay time; otherwise, the adjustment signal from the time-offset detector is used. As discussed above, the circuit of Figure 2 does not have this feature. Therefore, claim 7 is patentable over the circuit of Figure 2.

Claims 8-14 depend from claim 7 and are therefore patentable for at least the reasons stated above.

Independent claim 15 recites a method of providing a delay adjustment signal for controlling a delay time. The method includes generating a first adjustment signal, generating a second adjustment signal by "applying a noise-compensating condition to the first adjustment signal," generating a locking signal, and selecting one of the first and second adjustment signals as the delay adjustment signal, depending on the state of the locking signal. As discussed above, the circuit of Figure 2 does not perform these steps. For instance, no locking signal is generated, and a noise-compensated signal is always used as the delay adjustment signal. Therefore, claim 15 is patentable over the circuit of Figure 2.

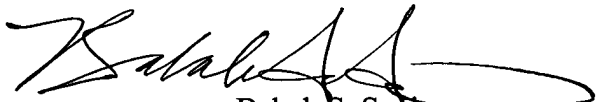
Claims 16-18 depend from claim 15 and are therefore patentable for at least the reasons stated above.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



Babak S. Sani
Reg. No. 37,495

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
BSS:lo
SF 1325902 v1

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